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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/491,302	01/25/2000	John D. Geissinger	55271USA6A	8370

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3M INNOVATIVE PROPERTIES COMPANY
PO BOX 33427
ST. PAUL, MN 55133-3427

EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/491,302	GEISSINGER ET AL.	
	Examiner	Art Unit	
	Paul E. Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 8-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 4 and 8 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller et al. (USPAT 5844168, Schueller) in view of Brandt et al. (USPAT 6068782, Brandt).

With regard to claim 1, Schueller discloses in figures 7 – 7b an electronic package. Schueller discloses in figures 7 – 7b a conductive trace layer (720b) having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads. Schueller discloses in figures 7 – 7b a dielectric substrate (720a) mounted on the first side of the conductive trace layer. Schueller discloses in figures 7 – 7b and column 8, lines 42 – 44 an embedded capacitor (bottom layer of 710, top layer of 700, and the bottom layer of 700) having a capacitance including a first conductive layer (bottom layer of 710), a second conductive layer (bottom layer of 700) and a layer of dielectric material (top layer of 700) made of a non-conductive polymer (polyimide, top layer of 700) disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer (725). It is inherent in the method of Schueller that the bottom layer of 710, top layer of 700, and the bottom layer of 700 form a capacitor because this configuration is the definition of a capacitor. Schueller is silent to teaching a specific

capacitance and a dielectric material made of a non-conductive polymer blended with high dielectric constant particles. Brandt teaches in column 4, lines 18 – 41 and column a suitable dielectric material made of a non-conductive polymer blended with high dielectric particles. Brandt further teaches in column 6, lines 44 – 60 a capacitor with this dielectric layer having a capacitance of 200 nF/sq.cm (500 pF is equivalent to 50 nF, (50 nF)/(0.25 cm^2) = 200 nF/cm^2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric material and capacitance of Brandt in the method of Kling in order to tune the electronic properties of a capacitor component as stated by Brandt in column 4, lines 22 – 41. It further would have been obvious to one of ordinary skill in the art at the time of the present invention to use a capacitance of from about 1nF/sq.cm to about 100 nF/sq.cm in order to optimize the capacitance, and because Brandt teaches optimization in column 4, lines 37 – 41 (also see MPEP 2144.05). Schueller discloses in figures 7 – 7b a plurality of interconnect regions (741 and 742) extending through the first conductive layer and the dielectric material layer of the capacitor. Schueller discloses in figures 7 – 7b an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected (750) to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected (751) to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

With regard to claim 2, Brandt teaches in column 2, lines 30 – 33 wherein an embedded capacitor has the first electrode maintained at a first reference voltage and wherein the second

electrode is maintained at a second reference voltage different from the first reference voltage. It is well known in the art that power and ground planes are maintained at reference voltages. Further, this is an intended use recitation that bears no patentable weight in a device claim.

With regard to claim 3, Schueller discloses in figures 7 – 7b and column 6, lines 28 – 30 an electrically conductive stiffening member (310) attached to the second conductive layer of the capacitor by a second adhesive layer (325).

With regard to claim 4, Schueller discloses in figures 7 – 7b a device receiving region (directly under 315) extending through the dielectric substrate, the conductive trace layer and the capacitor, and further comprising an electronic device (315) attached to the device receiving region on the stiffening member by a third adhesive layer (portion of 310b between 315 and 310, as labeled in figure 3).

With regard to claims 8 – 9, as discussed in the rejection of claim 1 above, Schueller and Brandt obviously teach the capacitor has a capacitance of 15 nF/sq.cm. MPEP 2144.05 states that the optimization of ranges within the prior art conditions, or through routine experimentation is obvious. It would have been obvious to one of ordinary skill in the art to use a capacitor that has a capacitance of about 2 nF/sq.cm. to about 30 nF/sq.cm because the optimization of ranges would have been obvious through routine experimentation in Schueller and Brandt.

With regard to claim 10, as discussed in the rejection of claim 1 above, Schueller and Brandt obviously teach the capacitor has a capacitance of at least 30 nF/sq.cm. MPEP 2144.05 states that overlapping ranges are obvious.

With regard to claim 11, Schueller discloses in column 7, lines 3 – 6 and Brandt teaches in column 4, lines 35 – 37 wherein the dielectric material of the capacitor has a thickness of 0.5 microns to about 30 microns. (see MPEP 2144.05, and note that 1mil = 25.4 microns).

With regard to claim 12, Brandt discloses in column 4, lines 18 – 41 wherein the dielectric material of the capacitor includes a metal oxide.

With regard to claim 13, Brandt discloses in column 4, lines 18 – 41 the high dielectric constant particles are formed from a material of lead zirconium titanate.

With regard to claim 14, Schueller discloses in figures 7 – 7b wherein the dielectric substrate includes a plurality of apertures, each one of the apertures being positioned adjacent to one of the interconnect region of the capacitor.

With regard to claims 15 – 16, Schueller discloses in figures 7 – 7b and column 7, lines 7 – 13 wherein the dielectric substrate includes a polyimide.

With regard to claim 17, Schueller discloses in figures 7 – 7b and column 2, lines 65 – 67 wherein the interconnect member is a solder plug (750 – 752).

With regard to claim 18, Schueller discloses in figures 7 – 7b wherein each interconnect pad is a solderball pad (340).

With regard to claim 19, Schueller discloses in figures 7 – 7b wherein the dielectric substrate has an aperture (portion filled by 365 in figure 7b) extending therethrough adjacent to each solderball pad.

Response to Arguments

3. Applicant's arguments filed January 27, 2005 have been fully considered but they are not persuasive.

4. With regard to applicant's argument that "the cited references do not provide a motivation or suggest for embedding a capacitor having a capacitance of from about 1nF/sq.cm. in the structure of Schueller," it should be noted that a capacitor is already embedded in the structure of Schueller and proper motivation has been provided as to how this capacitor may have a capacitance from about 1nF/sq.cm. While Schueller does not specifically state that the capacitor structure is used as a capacitor, the structure itself will still have capacitance and therefore function as an embedded capacitor. While a capacitance of from about 1nF/sq.cm. is common in capacitors, Schueller does not mention the particular capacitance of the embedded capacitor. Brandt is used for this feature and proper motivation is provided therefrom. Therefore, applicant's arguments are not persuasive and the rejection is proper.

5. In response to applicant's argument that "nowhere does Schueller indicate that it is using, or seeks to use, its metal and dielectric layers as a capacitor," a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re*

Otto, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). It should be noted that capacitance will exist in the capacitor structure of Schueller and thus it would be considered, by an ordinary artisan, a capacitor. In this case, the claimed intended use as a capacitor of a structure having capacitance does not define the present invention over the identical capacitance structure of Schueller. Therefore applicant's arguments are not persuasive and the rejection is proper.

6. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Specifically in response to applicant's argument that "there would be no motivation based on the teachings of Schueller to 'tune the electrical properties' of the layers in the Schueller article to make them into a capacitor having a capacitance," it is noted that Schueller already has a capacitor and thus nothing is made into a capacitor in the combination. Brandt is the source of the motivation to "tune the electrical properties" of the capacitance structure of Schueller. Applicant has not argued why the combination of Schueller with Brandt is not proper. Therefore, applicant's arguments are not persuasive and the rejection is proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II